
Journal of Engineering Technology and Applied Physics

The Design of Low Power Op-amp for Biomedical Application

Ameerul Asyraf Nasir, Chu Liang Lee*, Kah Yoong Chan, Lini Lee and C Senthilpari

Faculty of Engineering, Multimedia University, Cyberjaya, Malaysia.

*Corresponding author: clee@mmu.edu.my, ORCID: 0000-0001-5226-6837

<https://doi.org/10.33093/jetap.2024.6.1.4>

Manuscript Received: 30 July 2023, Accepted: 25 August 2023, Published: 15 March 2024

Abstract - This work presents a low-power operational amplifier (op-amp) circuit design which optimized and tailored specifically for biomedical circuit application in low power environment. The proposed op-amp design incorporates the folded cascode differential amplifier technique with a low voltage supply 1.2 V, utilizing current biasing, current mirrors, and adopted low-power circuit topologies. AC and DC analysis are carried out to analyse the performance of the proposed design. Extensive simulations executed using industrial standard EDA tool have validated the circuit design, and demonstrated a gain of 70.94 dB, UGBW of 4.90 MHz, GM of 52.70 dB, PM of 82.02 degrees, PSRR of 82.77 dB, CMRR of 100.78 dB, and total power dissipation of only 28.07 μ W. Low power consumption is essential for biomedical circuit applications, and the result shows a significant power reduction without compromising other performance parameters. The proposed op-amp circuit design is suitable to be implemented in low-power and high-performance biomedical devices.

Keywords—Operational amplifier, Low-power design, Biomedical applications, Folded cascode, Healthcare devices

I. INTRODUCTION

Operational amplifiers (op-amps) are essential components in analog electronic circuits. It was widely use in biomedical applications where their main implementation is to amplify biopotential signals in the human body for an accurate diagnosis, monitoring, and therapy [1].

Amplifying biopotential signals poses unique challenges due to their modest amplitudes and susceptibility to environmental noise. To address these challenges, low-power op-amps with wider bandwidths and high gains are necessary to ensure accurate signal amplification while maintaining low noise levels. Additionally, stability, precision, and low power consumption are crucial factors in biomedical applications,

particularly in implantable sensors and portable medical devices [2].

This work focuses on designing a low-power op-amp specifically tailored for biomedical signal processing. The design incorporates various techniques, including current mirror topologies, biasing circuit optimization, and low-power amplifier architectures, to minimize power consumption without compromising performance. The op-amp's key parameter, such as gain, unity gain bandwidth (UGBW), gain margin (GM), phase margin (PM), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and power consumption, are carefully analysed and optimized to meet the requirements of biomedical applications.

To validate the effectiveness of the proposed design, extensive simulations are conducted using industrial standard EDA simulation tool. These simulations ensure that the low-power op-amp design achieves the desired amplification performance while consuming minimum power. By providing precise signal amplification and power savings, this work contributes to development of low-power, high-performance biomedical devices, benefiting both patients and healthcare professionals.

II. FOLDED CASCODE OPERATIONAL AMPLIFIER

Figure 1 shows the basic structure of a folded cascode op-amp which comes from the folded cascode topology. The n-channel cascode active load from the different pair is folding down and changing the MOSFET to the p-channel transistors [3]. The advantage of the topology of this design is that it is able to provide high output swing and steering in low voltage circuit. Nonetheless, it still has a slightly higher noise compared to the other topology such as telescopic op-amp.

The folded cascode amplifier is a single-pole operational amplifier with large output swing and has higher gain compared to the ordinary op-amp.

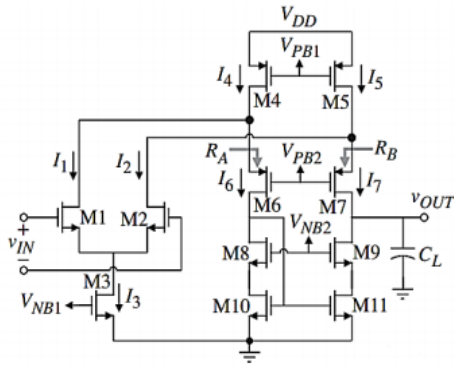


Fig. 1. Basic topology of folded cascode op-amp.

III. BIOMEDICAL OP-AMP SPECIFICATION

Op-amp circuit in biomedical applications require precise and reliable signal amplification to extract useful data from physiological measurements. Therefore choosing the proper operational amplifier (op-amp) characteristics is essential. The minimal gain criterion is an important consideration. A larger gain is preferred due to their typically modest amplitudes to amplify biomedical signals to a level at which they can be measured. This improves the signal-to-noise ratio, enabling the detection of minute physiological changes.

The bandwidth of the op-amp is another crucial factor. Depending on the precision of the measurement, biomedical signals may span a broad frequency range. Wide bandwidth is required to effectively capture the entire spectrum of these signals without adding distortion or frequency roll-off.

Two stability parameters, gain margin (GM) and phase margin (PM), are essential for minimising unwanted oscillations and preserving a steady output. Biomedical amplification circuits require enough GM and PM to maintain consistency and predictability regardless of the load impedance or feedback network.

In biomedical applications, common-mode interference can be a source of significant concern. The common-mode rejection ratio (CMRR) measures the op-amp's ability to reject unwanted signals simultaneously at both inputs. The precision of differential signal amplification is important, while common-mode noise, such as interference from power lines or electrode defects have to be rejected effectively [4].

The power supply rejection ratio (PSRR) is crucial in biomedical applications. The precision of signal amplification may be affected by power supply fluctuations or noise. By having a high PSRR, an operational amplifier can resist variations in the power supply voltage and maintain stable amplification performance. Power consumption must be minimised for portable and battery-powered biomedical devices to have extended battery lives and be more mobile.

Low-power op-amps with low quiescent current (Iq) and adequate power supply voltage ranges should be selected to

maximise power efficiency without compromising performance. By paying close attention to fundamental op-amp properties such as gain, bandwidth, stability, CMRR, PSRR, and power consumption, designers can provide accurate and dependable amplification of biomedical signals, thereby enabling precise analysis and interpretation of physiological data.

Table I shows the minimum specification requirements of design based on the biomedical specification and existing op-amp [1, 5–9]. In this work, a more stringent requirement of specification is proposed, as shown in Table I in order to obtain a better performance with low supply voltage.

Table I: The specification of circuit design for biomedical application.

Specification	Minimum requirement	Proposed requirement
Gain	Sufficient gain (> 60 dB)	> 70 dB
Unity Gain Bandwidth (UGBW)	Wide range (>MHz)	> 4 MHz
Bandwidth (BW)	> 1 kHz	> 1 kHz
Gain Margin (GM)	> 10 dB	> 50 dB
Phase Margin (PM)	> 45 degree	> 70 degree
Power Supply Rejection Ratio (PSSR)	≥ 60 dB	≥ 80 dB
Common Mode Rejection Ratio (CMRR)	≥ 80 dB	≥ 80 dB
Power Consumption	< 1 mW	< 30 μW

IV. PROPOSED CIRCUIT DESIGN

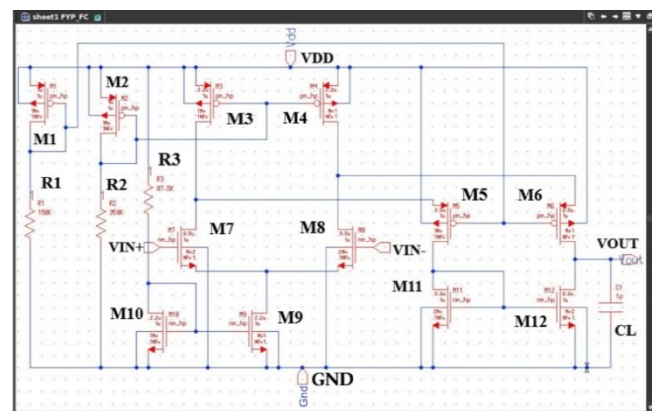


Fig. 2. The proposed circuit design of folded cascode op-amp.

In Fig. 2, M7 and M8 comprise the differential input pair, and M5 and M6 are the cascode transistors. Each M7 and M8

is a common source amplifier itself, forming a differential amplifier for input signals. The gate terminals of M_5 and M_6 are connected to a constant dc voltage and are at signal ground. M_1 is built as a current source in diode connected condition, where its $V_{DS} = V_{GS}$. It is used to bias the M_5 and M_6 . The gate voltage, V_G of M_5 and M_6 is equal to the voltage drop at R_1 (V_{R1} or $V_{DD} - V_{SG1}$). Thus, for differential input signals, each transistor pair of M_7 - M_5 and M_8 - M_6 functions as a folded cascode amplifier. A constant-current source biases differential pair to operate well.

The constant-current source, also known as the tail current for operating the differential pair branch, depends on the well-being of transistors M_9 . This constant current is essential as it helps establish a reliable operating point for the differential pair and consistent performance. The current mirror topology must be implemented for M_9 and M_{10} to ensure a consistent and precise current level. The transistors of M_{10} would be diode-connected as $V_{DS} = V_{GS}$. The gate voltage, V_G of transistors, M_9 is equal to the V_{GS} of M_{10} as it biased the same voltage. Due to the current mirror connection, M_9 will convey the same amount of current as the current source. Thus, each of M_7 and M_8 is operating at a biased current, $\frac{I_{D9}}{2}$.

A node equation at each of their terminals shows that the bias current of each of M_5 and M_6 are $I_{D3} - \frac{I_{D9}}{2}$ and $I_{D4} - \frac{I_{D9}}{2}$. The differential output current from M_7 - M_8 and M_3 - M_4 is fed to the source terminal of M_5 and M_6 . Sizing and appropriate calculation must ensure that M_3 - M_4 is in the saturation region and not affecting the headroom's voltage. M_{11} and M_{12} are cascode current mirrors used to suppress the effect of channel-length modulation. M_{11} is a diode-connected to guarantee the M_{12} also operates in a saturation region. This current mirror transforms the double-ended output into a single-ended output without any additional components needed [3].

The entire capacitance at the output node is indicated by the term capacitance C_L . It consists of the internal transistor capacitances, any actual load capacitance, and perhaps a further capacitance that was purposefully included for frequency adjustment. To accomplish the appropriate frequency correction, additional capacitance is frequently not necessary because the load capacitance will often be sufficiently large. The load capacitance helps with frequency compensation, unlike the two-stage circuit that needs a separate compensation capacitor (C_C). Transistor M_9 supplies the continuous current used for biasing the differential pair, while M_3 and M_4 supply the constant bias currents, I_{D3} and I_{D4} .

V. SIZING AND SMALL CIRCUIT CONFIGURATION OF PROPOSED DESIGN

The operating mode of transistor is calculated by using drain current equation as shown in the Eq. (1), where μ_0 is a mobility of the carrier in silicon (electron, μ_n or hole, μ_p) and C_{ox} is capacitance oxide. The value $\mu_n C_{ox}$ and $\mu_p C_{ox}$ are $102\mu A/V^2$ and $181\mu A/V^2$. The transistor size is rounded into a single decimal place as it would make the layout process

easier as shown in Table II and Table III. The compensation capacitor is set to be 1 pF as Miller's compensation. This compensation ensures the design's stability and helps in pole-splitting as it increases the phase margin (PM). To build and design low-power op-amp, V_{DD} is set to be 1.2 V.

$$I_D = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \tag{1}$$

Table II: The size of the transistor in folded cascode circuit design.

Transistors	Multiply M	Size (W/L)
M_1	1	1.0
M_2	1	1.0
M_3	1	2.2
M_4	1	2.2
M_5	1	0.5
M_6	1	0.5
M_7	2	0.5
M_8	2	0.5
M_9	1	2.2
M_{10}	1	2.2
M_{11}	2	0.8
M_{12}	2	0.8

Table III: The value of the impedances in folded cascode circuit design.

Impedance R / Capacitance C	Value
R_1	150 Ω
R_2	350 Ω
R_3	87.5 Ω
C_L	1 pF

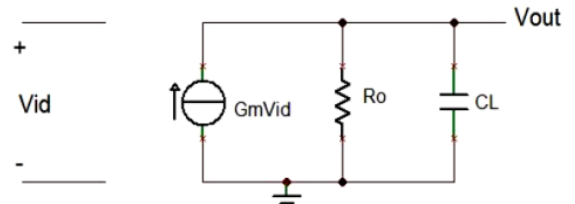


Fig. 3. The small circuit configuration of proposed circuit design.

A half-circuit analysis on the differential amplifier circuit needs to be performed to analyse the small-signal configuration and determine important parameters such as pole and zero in the circuit design. The small signal

equivalent circuit configuration of this circuit design is shown in Fig. 3. G_m is the total transconductance of the half circuit and V_{id} is the input differential voltage of the half circuit, R_0 is the output impedance at the output node, and C_L is an output load capacitance. The half-circuit may help to determine the pole and zero of the first stage of the op-amp circuit, which would allow further improvement on the performance of the op-amp. The half-circuit structure is shown in Fig. 4.

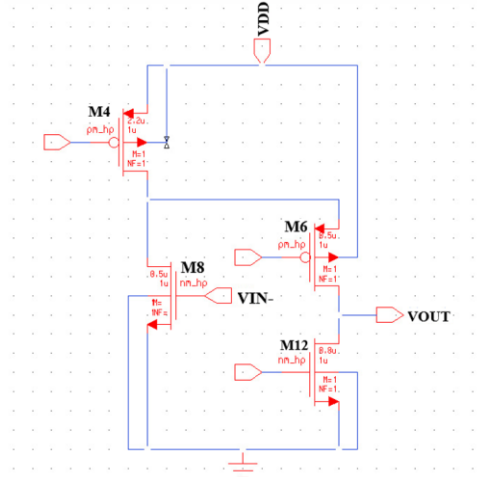


Fig. 4. The half- circuit configuration of proposed circuit design.

With the half-circuit analysis:

$$A_v = \frac{-g_{m8}g_{m6}(R_6 || R_8 + R_4)}{1+g_{m12}R_{12}} \quad (2)$$

$$A_v = \frac{V_o}{V_{in}} \quad (3)$$

$$\frac{V_o}{V_{in}} = \frac{-g_{m8}g_{m6}(R_6 || R_8 + R_4)}{1+g_{m12}R_{12}} \quad (4)$$

Analyse the pole and zero position of the circuit design:

$$\frac{V_o}{V_{in}} = \frac{A_{DC}(1-\frac{s}{z})}{1+s(\frac{1}{p_1}+\frac{1}{p_2})+s^2(\frac{1}{p_1p_2})} \quad (5)$$

The dominant pole:

Note that the $\frac{1}{p_2}$ is absent so that it can be neglected.

C_L is at the output node (dominant pole) of the design.

$$p_1 = \frac{1}{g_{m12}R_{12}} \quad (6)$$

$$p_1 = \frac{1}{g_{m12}R_{12}C_L} \quad (7)$$

The zero: $Z = 0$ (8)

DC gain, A_{DC} :

$$A_{DC} = -g_{m8}g_{m6}(R_6 || R_8 + R_4) \quad (9)$$

VI. RESULT AND DISCUSSION

The proposed folded cascode op-amp has been simulated using industrial standard EDA tool. The performances parameter values of the op-amp are verified through the DC and AC analysis. Figure 5 shows the AC analysis configuration with appropriate DC level. The performance parameter of gain, unity gain bandwidth (UGBW), bandwidth, phase margin (PM), PSRR, CMRR, and power dissipation are obtained using AC analysis. Figure 6 shows the operating point of transistors in the op-amp circuit obtained by DC analysis.

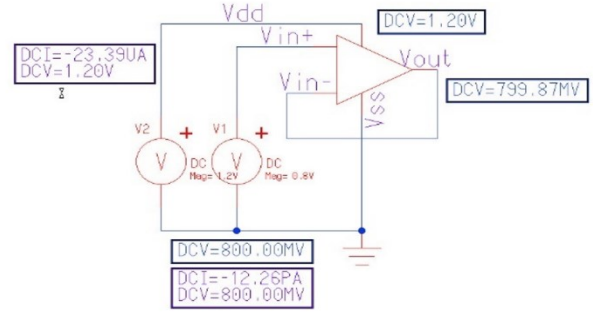


Fig. 5. The DC analysis configuration.

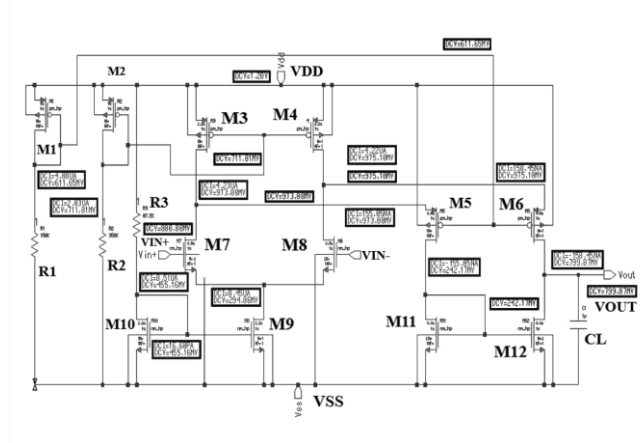


Fig. 6. The operating region of transistors in DC analysis.

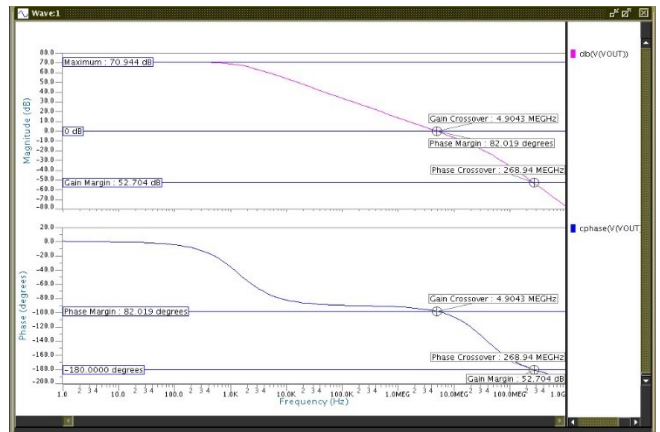


Fig. 7. The bode plot of the circuit design in AC analysis.

Op-amps require specific biasing conditions to function within their linear range. This DC configuration has determined the operating region of the transistors in the circuit

design. Figure 6 demonstrates that all transistors are saturated when $V_{GS} > V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH}$. The V_{DS} of the transistor must exceed the overdrive voltage to operate in the saturation region. This saturation operating region in operational amplifiers contributes to the overall circuit's minimal distortion. The output impedance will be minimal when transistors operate in the saturation region. This means it can effectively drive low-impedance loads, enhancing signal transfer and reducing signal loss.

Figure 7 depicts the bode plot generated by the AC analysis performed on the folded cascode op-amp circuit design. The efficacy of the circuit design can be analysed using this bode plot. The circuit's differential gain (A_v) is calculated to be 70.94 dB. This circuit design yields a high gain, which is advantageous for biomedical applications. High differential gain may aid in maintaining the signal's accuracy without introducing noise distortion.

PM, GM, and unity gain bandwidth (UGBW) are additional data that can be examined using the bode plot. This circuit yields a bandwidth with a unity gain of 4.90 MHz ($UGBW = \text{Gain} \times \text{Bandwidth}$). The unity gain bandwidth is the frequency at which the open loop gain of the operational amplifier falls to 0 dB. Op-amps are frequently used in filter circuits in biomedical applications to eliminate noise and undesirable frequency components.

The gain margin (GM) is 52.70 dB, and the phase margin (PM) is 82.02 degrees. Biomedical applications frequently deal with small, delicate signals susceptible to distortion and corruption. The higher PM ensures stability by permitting a larger phase shift margin between the op-amp's input and output. It demonstrates that the circuit design can reduce common-mode noise and produce a cleaner output signal. The operational amplifier is exceedingly stable when its phase margin (PM) exceeds 60 degrees [10].

Next, high GM in the circuit design ensures the robustness of the op-amp by allowing it to manage variations such as load and temperature effectively. Adequate capacitive load must be applied in the design as it would sacrifice the unity gain bandwidth while increasing the phase margin [9]. Therefore, in biomedical applications, finding a balance between the gain, bandwidth, and phase margin is important for flawless operation.

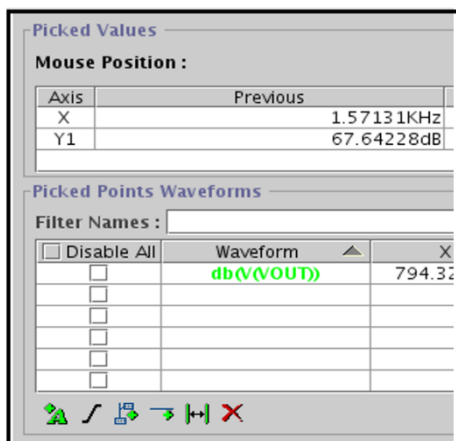


Fig. 8. The bandwidth (f_{-3dB}) of the circuit design in AC analysis.

Figure 8 shows values captured based on the simulated result. Due to the limitation on capturing precise value on the simulation tool, the bandwidth frequency at -3 dB gain drop can only be obtained at 67.64 dB instead of 67.94 dB. Therefore the bandwidth value of 1.57 kHz as shown in Fig. 8 supposed to be slightly lower. In order to obtain a more accurate bandwidth value, Eq. (10) is used and the calculated value is 1.39 kHz. Equation (10) is given as below:

$$BW = \frac{UGBW}{Gain} \tag{10}$$

This bandwidth is sufficiently broad and compatible for use in various biomedical applications. In biomedical applications, a wide bandwidth is required to ensure accurate signal amplification and maintain signal integrity, as it prevents the signal's essential details and characteristics from being lost during amplification.

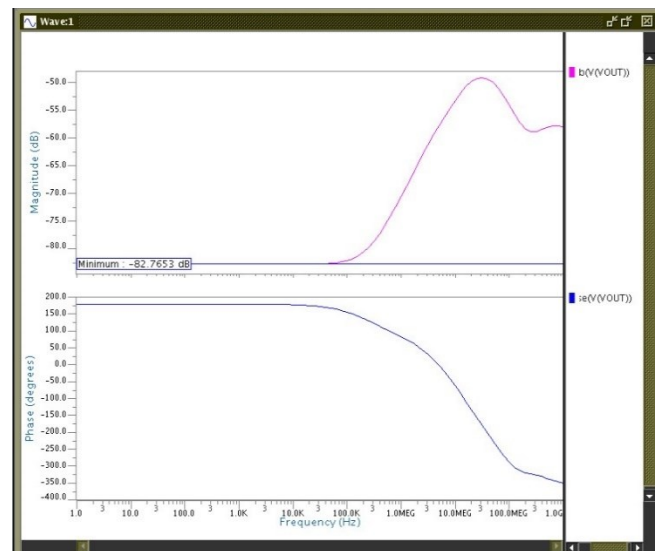


Fig. 9. The PSRR result of circuit design in AC analysis.

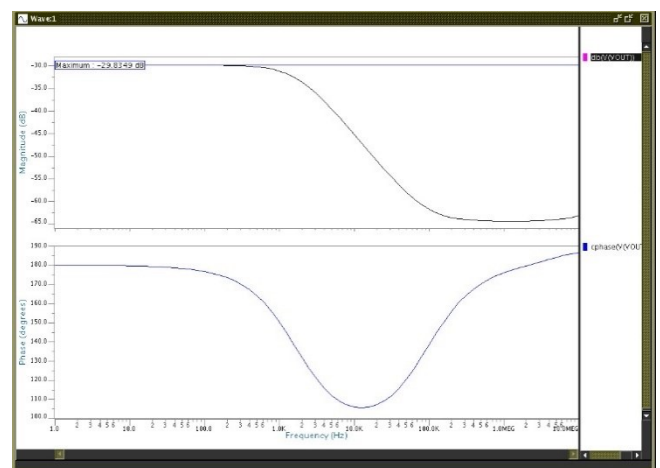


Fig. 10. The result of common-mode gain (A_{cm}) in AC analysis.

The PSRR for the circuit design is -82.77 dB, as depicted in Fig. 9. The result demonstrates the circuit design has an exceptionally high-power supply noise rejection. A high PSRR ensures that the op-amp's output is relatively unaffected by power supply disturbances, allowing for the

amplification of signals with reliability and precision. Maintaining a consistent power supply in biomedical applications is difficult due to noise and electromagnetic interference [11].

$$CMRR = 20 \log_{10} \left(\frac{A_{DM}}{A_{CM}} \right) \quad (11)$$

According to Fig. 10, the common-mode gain is -29.83 dB, which indicates that the op-amp effectively rejects the common-mode signal. Based on the Eq. (11) and simulated result, calculation concluded that the CMRR of this circuit design is 100.78 dB, which is sufficient for biomedical applications. With a high CMRR, accuracy and signal integrity can be maintained because the CMRR effectively rejects common-mode signals and reduces the influence of external interference. It also mitigates grounding issues in the biomedical system's operational amplifier. High gain and high CMRR op-amps are essential for analog front-end circuits used in biomedical applications [4].

```
X_FYP_FC11.N$67 711.8097M
TOTAL POWER DISSIPATION: 28.0651U WATTS
Connecting to JWDB server, please wait...
connected to wdb server : -jwdbhost MentorEDA -jwdbport 43171
```

Fig. 11. The total power dissipation of circuit design.

Table IV: The comparison result of circuit design for biomedical application.

Specification	References				This work
	[5]	[6]	[7]	[9]	
Technology (nm)	180	180	180	180	120
Power Supply (V)	1.80	1.80	1.80	1.8	1.20
Gain (dB)	72.54	84.34	64.8	54	70.94
UGBW (MHz)	16.65	6.34	1.09	-	4.90
Bandwidth (kHz)	-	-	-	55	1.39
Gain Margin, GM (dB)	-	-	-	-	52.70
Phase Margin, PM (degrees)	61.42	68.89	61	88	82.02
PSRR (dB)	-	-	-	-	82.77
CMRR (dB)	60	128.4	110	-	100.78
Power Consumption (μ W)	1003	143	402	450	28.07

$$P_{static} = V_{dd} \times I_{static} \quad (12)$$

As illustrated in Fig. 11, the total power dissipated by the circuit design is 28.07 μ W. The calculation also can be verified using Eq. (12) and the simulated result. The proposed design's power consumption is less than the proposed specification. It is essential to have a low-power op-amp with high performance, as many trade-offs must be considered during the design process. In biomedical applications, it is necessary to have minimal power dissipation and reduced heat generation for longer battery life in biomedical devices. It also increased the system's dependability by increasing the durability of biomedical devices and ensuring their consistent performance over an extended period.

The comparison between simulated result in this work and the previous researches are shown in Table IV. The result of this work shows a high gain for biomedical application although the voltage supply has been reduced significantly. The design also has an outstanding GM and PM in which indicates a great stability and robustness. CMRR and PSRR show an extraordinary outcome as the data prove that the design is less prone to distortion or interference. However, due to the trade-off, the design has low bandwidth in which can be improved further. By and large, this design has shown a better optimized and improved results with low voltage supply and tremendous reduction in power consumption.

VII. CONCLUSION

This work highlighted the significant of considering important application requirements and challenges in biomedical applications specification, such as low power consumption, accurate signal amplification with high gain, and stability with improved phase margin. The voltage supply for the op-amp circuit is 1.2 V. The folded cascode circuit technique is being adopted in this work to attain the biomedical application circuit requirements.

In conclusion, the work has successfully contributed to the development of a low-power op-amp design using folded cascode circuit technique for biomedical applications. The op-amp circuit design obtained a power consumption of 28.07 μ W, which is a significant reduction in total power consumption compared to previous researches. In the other hand, it also obtained some improvement on parameters such as CMRR, UGBW, gain and phase margin. Extensive simulations executed using industrial standard EDA tool have validated the circuit design, demonstrating a gain of 70.94 dB, UGBW of 4.90 MHz, GM of 52.70 dB, PM of 82.02 degrees, PSRR of 82.77 dB, and CMRR of 100.78 dB. This op-amp design has the potential to benefit a wide range of circuit implementation in biomedical applications, including medical instruments, wearable devices, implantable sensors, and bio-signal processing systems.

REFERENCES

- [1] W. M. E. A. W. Jusoh and S. H. Ruslan, "Design and Analysis of Current Mirror OTA in 45 nm and 90 nm CMOS Technology for Bio-Medical Application," *Bullet. Electr. Eng. and Inform.*, vol. 9, no. 1, pp. 221–228, 2020.
- [2] P. Nagarajan, M. Srividhya and P. G. Scholar, "An Effective Low Power High Gain Op-Amp Design for Bio-Medical Application," *Int. J. Pure and Appl. Math.*, vol. 120, no. 6, pp. 2197–2208, 2018.

- [3] L. C. Sing, N. Ahmad, M. M. Isa and F. A. S. Musa, "Design and Analysis of Folded Cascode Operational Amplifier Using 0.13 μm CMOS Technology," in *AIP Conf. Proc.*, 2203, No. 020041, pp. 1-5, 2020.
- [4] K. N. Abhilash, S. Bose and A. Gupta, "A High Gain, High CMRR Two-Stage Fully Differential Amplifier Using g_m/I_d Technique for Bio-medical Applications," in *Asia Pacific Conf. Postgraduate Res. Microelectron. and Electron.*, pp. 40-45, 2013.
- [5] W. Jin, "Design and Analysis of Two Stage Op-Amp for Bio-Medical Application," *Asia-Pacific J. Converg. Res. Interchange*, vol. 3, no. 4, pp. 27-35, 2017.
- [6] K. Shashidhar, S. R. Ijjada and B. S. Naick, "Design and Implementation of CMOS Telescopic Op-Amp for Bio-Medical Applications," *Int. J. Simulation: Sys., Sci. & Technol.*, pp. 31.1-31.10, 2020.
- [7] K. J. Kiruthika and A. Beno, "High Gain Bio Signal Amplifier Design for Health Monitoring Applications," *Int. J. Res. & Develop. Technol.*, vol. 7, no. 4, pp. 857-860, 2017.
- [8] G.N. Rani, G. Gifita, M. Meenaksi, C. Gomathy, T. Gowsalaya, "Design and Analysis of CMOS Low Power OTA for Biomedical Applications," in *Proc. 4th IEEE Int. Conf. Recent Trends Electron., Inform., Comm. & Technol.*, Bengaluru, India, 17-18 May, 2019.
- [9] G. Prasad, "A Low Power, 54 dB Open Loop Gain, Folded Cascode CMOS Operational Amplifier Using 180 nm Technology," doi: 10.13140/RG.2.2.35075.50722, 2017.
- [10] G. Naresh Sagar, B. Anil Kumar and G. V. Subba Reddy, "Low-Power High-Gain Op-Amp with Cascoded Current Mirror Loads," in *Proc 5th Int. Conf. Electron., Comm. and Aerospace Technol.*, pp. 179-186, 2021.
- [11] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd Edn., McGraw-Hill Education, New York, 2017.