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Simulation Of Dual-Material Hetero-Double Gate Tunnel Field Effect Transistor (TFET) In Sub-Micron Region

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***Abstract* - To meet the performance requirements of low power mobile devices, a device with a high ION/IOFF ratio at low-VDD is needed. TFETs are gaining popularity due to their low subthreshold slope and high transconductance compared to MOSFETs. However, silicon-based TFETs have low on-state current, which limits their use in high-performance applications. To overcome this limitation, using a narrower band gap material like Ge can increase tunneling efficiency at the source side. Additionally, the larger ambipolar current associated with Si-TFETs can be reduced by considering a dual-material hetero-double-gate-dielectric (DM HDG) TFET. The main objective of this research is to propose and characterize a new TFET structure by considering the advantages associated with hetero structure and hetero-gate-dielectric TFETs, which realizes a device with an enhanced I_{ON} and a suppressed ambipolar current. The structure was fabricated with the addition of a hetero-dielectric Buried Oxide (BOX) on the doped substrate for the reduction of ambipolar current. We will adopt source-to-gate overlap technique to achieve desired subthreshold slope (SS). All the simulations were done by using 2-D TCAD simulator by Atlas Silvaco. The structure was optimized in terms of (I_{ON}/I_{OFF}) and other performance metrics and simulation results were compared with other available structures in the literature.**

Keywords*— *TFET, Leakage current, Transconductance, Simulation

I. Introduction

The downsizing of MOSFETs was formerly a successful method for enhancing circuit performance, but in the post-scaling era, short channel effects (SCEs) and higher leakage current have rendered it ineffective [1-2]. Researchers have suggested a wide range of non-planar structures in the literature [3-5], particularly multi-gate devices and devices made from other materials to replace the conventional CMOS technology [6-8]. The main difficulty is to suppress leakage current without compromising the ON current in the nanoscale era. Leakage current is a serious issue in the device that alters the stable performance of the device. Nanowire transistors have been suggested as a way to manage the leakage current [9–11]. Tunnel field-effect transistors (TFETs) are regarded as one of these.

One of these is the tunnel field-effect transistor (TFET), which is anticipated to displace planar MOSFETs in the future [12–14]. Even while TFETs have a reduced subthreshold slope (SS) at room temperature (60 mV/decade), they nevertheless have two major drawbacks: a lower ON current and a higher ambipolar current [14-17]. On the other hand, TFET with gate-drain overlap structure have been proposed to lower ambipolar current [7] at the cost of reduced chip density. The ON current of TFET device can be improved by utilising high k-dielectric material as a gate insulator [18] on the cost of increased Iamb. In the literature, hetero-dielectric gate (HDG) TFET is proposed to address these two drawbacks by utilizing SiO_2 at the drain to decrease ambipolar current and a high-k material partially near the source to boost the ON current.

In this paper, we have using Pseudo-2D method and studied the electrical behaviour of the DMHDG TFET devices in terms of surface potential, tunneling width, drain current and transconductance parameter after developing the compact close form of analytical expression for drain current [16]. We have ignored the source/drain depletion width due to heavy doping and quantum confinement effect due to silicon film thickness (> 3 nm). The present paper is

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organized as: Section II describes device structure of the model. Section III discusses the electrical behaviour of the proposed structure and at the end, we conclude the paper in section IV.

II. Device Structure

A. I. Structure of DMHDG TFET

The 2-D structure and coordinate system of the proposed N-type hetero-dielectric gate TFET (DMDG TFET) is shown in Fig. 1 [19].

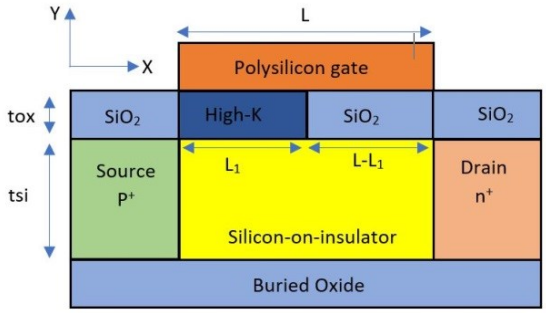

Fig. 1. Structure of DMHDG TFET.

The proposed structure has a hetero-dielectric gate, which means that the gate dielectric is composed of two different materials with different dielectric constants. The hetero-dielectric gate consists of a buried oxide layer (BOX) and a top dielectric layer, which are located between the metal gate and the low-k dielectric layer. The hetero-dielectric gate is designed to reduce the ambipolar current and enhance the on-state current of the device.

A. II Analytical Model

Pseudo-2D method was used to solve the Poisson equation as this method simplifies the solution of the Poisson equation and makes it computationally feasible.

By referring to Fig. 1, after neglecting the fixed carrier oxide charges, 2-D Poisson's equation, for the potential distribution $\psi_j(x,y)$ in the respective region, is given as [20]

$$\frac{d^2\psi_j(x,y)}{d^2x} + \frac{d^2\psi_j(x,y)}{d^2y} = -\frac{qN_a}{\varepsilon_{si}} \tag{1}$$

, where N_a is the channel doping concentration, j = 1, 2 represents the region I and region II respectively, ε_{si} is the silicon permittivity, $\psi_j(x,y)$ is the 2-D electrostatic potential in the region I and II measured with respect to Fermi potential respectively.

The 2-D electrostatic potential in the channel can be represented as follows by assuming a parabolic potential profile along the film thickness (i.e. along the y-direction),

$$\varphi_{j(x,y)} = a_0 + a_{j1}y + a_{j2}y^2 \tag{2}$$

, where a_{0j}, a_{j1} and a_{j2} are constants and function of x-only. The following Boundary Conditions (BCs) can be used to obtain these constants:

$$\left.\frac{d^2\varphi_{j(x,y)}}{dy^2}\right|_{y=0} = 0, \tag{3}$$

$$\varphi_{j(x,y)}\Big|_{y=\frac{t_{si}}{2}} = \phi_{sj(x)}, \tag{4}$$

$$\left.\frac{d^2\varphi_{j(x,y)}}{dy^2}\right|_{y=\frac{t_{si}}{2}} = -\frac{C_{ox1}}{\epsilon_{si}}\left[V'_{GSf_j} + \phi_{Sj(x)}\right] \tag{5}$$

, where $\phi_{Sj(x)}$ is surface potential, $V'_{GSf_j} = V_{GS} - V_{fb}$. V_{fb} is flat-band voltage which is given as $V_{fb} = \phi_m - \left[x + \frac{E_g}{2} + \frac{kT}{q}\ln(\frac{N_c}{n_i})\right]$

B. Tunneling Current

In non-local BTBT, tunneling charges start only when conduction band edge (CB) of source coincides with the valence band edge (VB) of the channel region [3]. The tunneling current can be obtained by integrating the Kane band-to-band tunneling (BTBT) generation rate over both radial and lateral directions tunneling volume as

$$I_{BTBT(S-C)} = q\iiint G_{BTBT}\, dxdydz \tag{6}$$

, where G_{BTBT} is the generation rate of the carriers and given as

$$G_{BTBT} = A_k E_{av}^D \exp\left(-\frac{B_k}{E}\right) \tag{7}$$

A_k and B_k are Kane's parameters dependent upon the effective tunneling mass, charge, the effective bandgap at the tunneling junction and Planck constant and their values are; A_k = 1.4 × 1020 $eV^{1/2}$ //cm.s.V^2 and B_k = 8.6 × 10^6 V/cm.$eV^{3/2}$, respectively, E_{av} is average electric field, E is the resultant field, and D is fitting parameter (its value is either 2 or 2.5 depending upon the nature of semiconductor material).

III. RESULTS AND DISCUSSION

The proposed analytical models are simulated for following values of the parameters; L = 50 nm, $t_{ox1} = t_{ox2}$ = 3 nm, t_{si} = 10 nm, V_{ds} = 0.7 V, N_s = 1020 /cm^3, N_d = 10^{18} /cm^3, N_c = 10^{16} /cm^3 unless and until specified.

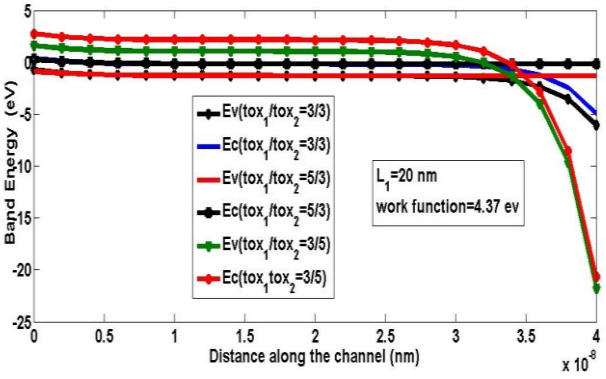

Fig. 2. Band diagram for various combination of oxide thicknesses in two regions.

From Fig. 2 above, the result shows that sharp band bending occurs for $t_{ox1} = 3$ nm and $t_{ox2} = 5$ nm due to reduction of equivalent oxide thickness which enhances the coupling between the gate and the channel junction. The surface potential change was observed to occur mainly within about 10 nm from the source-channel interface. This is entirely in the high-k region. The surface potential outside the tunneling space (mainly in the low-k region) changes little. This indicates that the tunneling is controlled only by the high-k dielectric and the drain has no effect on the tunneling current. This behavior allows for better control and optimization of the tunneling current, leading to improved transistor performance. By focusing on optimizing the properties of the high-k dielectric, such as its thickness and dielectric constant, the TFET can be designed to achieve specific performance targets such as low power consumption, high speed, or high gain.

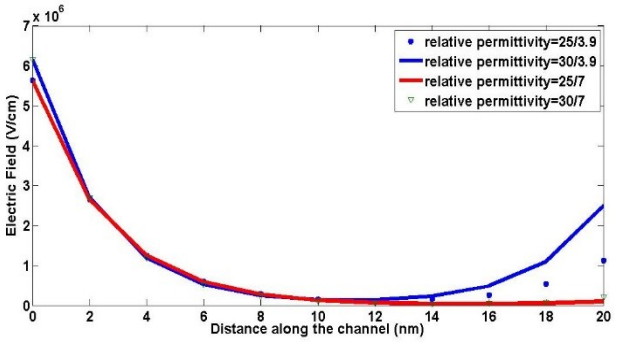

Fig. 3. Variation of the electric field along the channel for different dielectric constant (relative permittivity) combinations.

The lateral electric field decreases along the channel and reaches a minimum value in mid-range of the channel. Figure 3 shows the variation of the electric filed along the channel for different combinations of dielectric constants. We observed that electric field takes on a larger value when region I is occupied by high-k dielectric material.

By increasing the doping concentration ratio between the source and drain regions, the surface potential near the edge of the source end becomes steeper, improving the electrical characteristics at narrow tunneling width. Due to this phenomenon, the threshold voltage decreases irrespective of the channel length, as shown in Fig. 4.

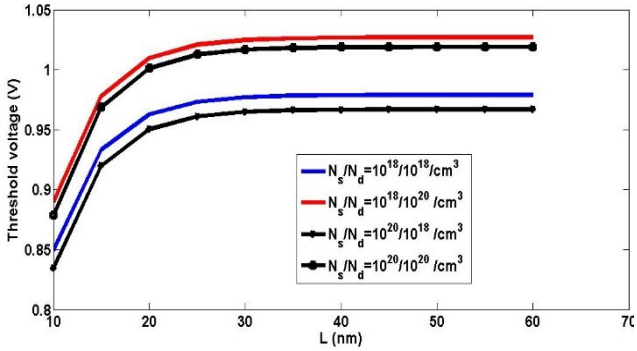

Fig. 4. Threshold voltage of DMHDG TFET device versus channel length for different concentrations combination in the source and drain regions.

As the length of region 1 decreases, conduction band becomes flatten, which makes band-to-band tunneling difficult and hence increases the threshold voltage. This is due to the conduction band becomes more flat, which makes it harder for band-to-band tunneling to occur, as shown in Fig. 5. It is observed that the larger tunneling length L_1 accumulates more charges, which resulting in a lower threshold voltage.

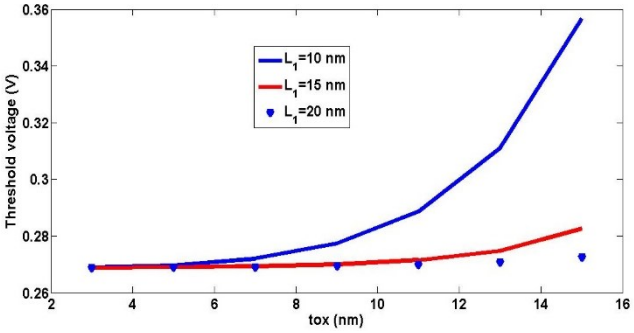

Fig. 5. Threshold voltage variation with t_{ox} for different tunneling length (L_1).

Table I shows the comparison results between the proposed threshold voltage model and the results of Ref. [20]. The results show a similarity between the proposed model and the results of Ref. [20], with minor differences that can be attributed to the dual-material gate structure used in the proposed model. The proposed model has shown to accurately predict the threshold voltage of the DMHDG TFET, which is a crucial parameter for device performance. This comparison validates the effectiveness and accuracy of the proposed threshold voltage model. For fair comparison, we adopted L = 50 nm, L_1 = 8 nm, k_{r2} = 21, k_{r1} = 3.9 and metal work functions of 4.0 eV and 4.4 eV as suggested in Ref. [21].

Table I: Threshold voltage comparison with reference results [20].

Φ_{m1} (eV)	Φ_{m2} (eV)	Threshold voltage (V)	
		Proposed	Ref [28]
4.0	4.0	0.349	0.34
4.4	4.4	1.10	0.74

Figure 6 shows a comparison of the results of the proposed model and those of the 2-D ATLAS simulator. The two results show excellent agreement with high-k gate materials due to controlled leakage current. This suggests that the proposed model is accurate and reliable in predicting the behavior of the high-k gate materials and can be used for further research and development of devices using these materials.

An important parameter for analog IC designers is transconductance (g_m), which measures the gain of the device. In general, the g_m value increases with increasing gate-source voltage due to the increased current capability of the device. The proposed DMHDG TFET yields larger g_m compared with the conventional TFET after a certain gate bias, as shown in Fig. 7. This is because the subthreshold swing of the proposed structure is lower than that of conventional TFET devices. As DMHDG TFET has a

heterostructure design, which involves using different materials with different bandgaps in the source and channel regions to enhance tunneling efficiency. The DMHDG TFET also has a double-gate structure with two different gate dielectrics, which allows for better gate control and reduces ambipolar current. These design features contribute to the improved g_m performance of the DMHDG TFET compared with conventional TFETs.

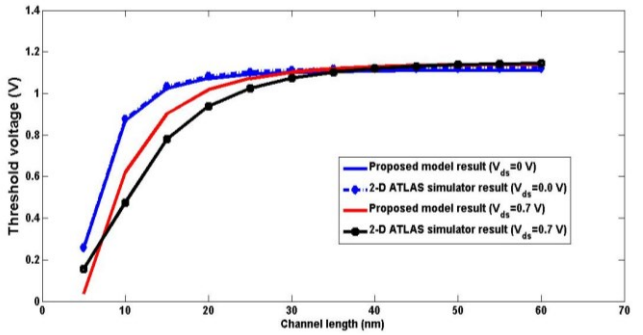

Fig. 6. Comparison of threshold voltage with proposed and 2-D ATLAS simulator.

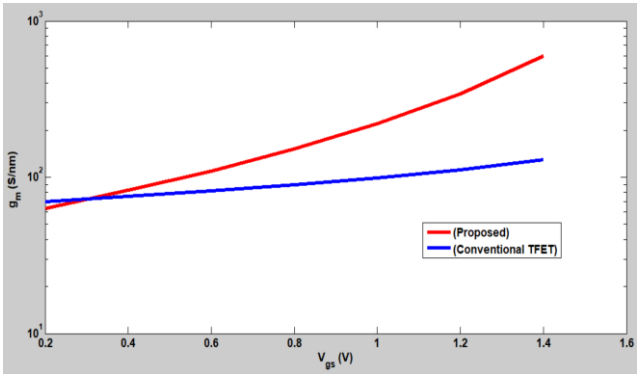

Fig. 7. Comparison of g_m value of DMHDG TFET device with conventional TFET (single gate).

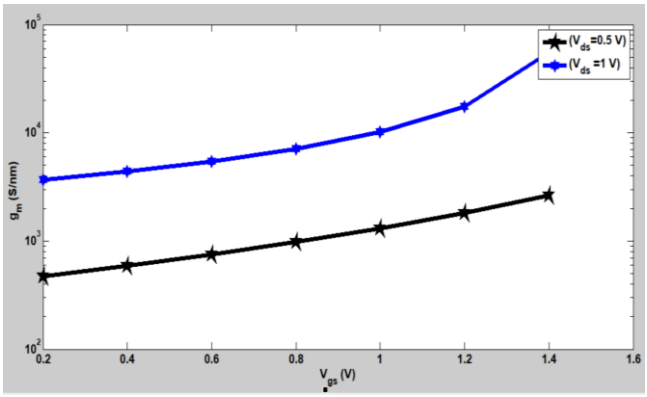

Fig. 8. g_m-versus V_{gs} for V_{ds}=0.5 V and 1.0 V.

The larger the drain voltage, the smaller the bipolar current in the proposed structure at any given gate bias, and hence the larger the transconductance value, as shown in Fig. 8. In the proposed DMHDG TFET structure, the presence of a hetero-dielectric buried oxide layer helps to reduce the ambipolar current, which is the sum of the forward and reverse currents. As a result, at any given gate bias, the structure already has a lower ambipolar current than a conventional TFET. When the drain voltage is increased, the reduction in bipolar current is even more significant, leading to an increase in transconductance value. This property makes the proposed structure attractive for analog IC designers who are looking to maximize the gain of their devices.

IV. CONCLUSION

This paper presents a comprehensive analysis of the DMHDG TFET device, which is a promising candidate for low-power and high-performance applications. The proposed tunnel width model is validated with 2-D TCAD simulation results, demonstrating good agreement. The device structure suppresses the ambipolar current and enhances the ON current while reducing short channel effects. Gate engineering is shown to be effective in reducing ambipolar current, increasing transconductance, and lowering the threshold voltage. Additionally, the proposed structure exhibits a lower subthreshold slope and larger transconductance value compared to the conventional TFET device. To further improve the performance of the proposed device, a combination of material engineering and thinner source gate oxide can be used. Overall, this paper provides important insights into the design and optimization of DMHDG TFETs for future low-power and high-performance electronic applications.

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